VMMK-1218
Application Information

Application Note 5385

Introduction

The Avago Technologies VMMK-1218 is a low noise enhancement mode PHEMT designed for use in low cost commercial applications in the VHF through 18 GHz frequency range. The small 0402 size makes the device very appealing where space is limited. The high gain and low noise figure of the 400-micron gate width of the VMMK-1218 makes the device particularly attractive kΩ for applications at VHF frequencies and higher. Higher gain at microwave frequencies comes with higher gain at VHF frequencies. As with all microwave FETs, certain precautions must be taken to insure broad band stability is achieved. More on this later.

The advantage of an enhancement mode PHEMT over a depletion mode PHEMT is that biasing the device is simplified by not requiring a negative power supply to bias the gate. The concern over sequencing the gate and drain voltages with a depletion mode device are non-existent with an enhancement mode device. Compared to a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Therefore, a negative power supply voltage is not required for an enhancement mode device. Biasing an enhancement mode PHEMT is much like biasing the typical bipolar junction transistor. Instead of a 0.7 V base to emitter voltage, the VMMK-1218 enhancement mode PHEMT requires a nominal 0.58 V potential between the gate and source for a nominal drain current of 20 mA.

Matching Networks

The techniques for impedance matching an enhancement mode device are very similar to those for matching a depletion mode device. The only difference is in the method of supplying gate bias. S-parameters and noise parameters for various bias conditions are listed in this data sheet. The circuit shown in Figure 1 shows a typical LNA circuit. (Consult the Avago Technologies web site for application notes covering specific designs and applications). High-pass impedance matching networks consisting of L1/C1 and L2/C2 provide the appropriate match for noise figure, gain, input return loss and output return loss. The high pass structure also provides low frequency gain reduction which can be beneficial from the standpoint of improving out-of-band gain rejection. The lumped element approach to impedance matching works well up to 5 to 6 GHz. Above this frequency range, L1 and L2 are often replaced with microstrip equivalents.

Capacitors C3 and C4 provide a low impedance in-band RF bypass for the matching networks. Resistors R3 and R4 provide a very important low frequency termination for the device. The resistive termination improves low frequency stability by providing a resistive termination for the device's low frequency gain. The ability of R3 and R4 to provide low frequency stability is based on C3 and C4 being no larger in value than absolutely necessary to provide an in-band bypass. Capacitors C5 and C6 provide the RF bypass for resistors R3 and R4. Their value should be chosen carefully as C5 and C6 also provide a termination for low frequency mixing products. These mixing products are as a result of two or more in-band signals mixing and producing third-order in-band distortion products. The low frequency or difference mixing products are terminated by C5 and C6. C5 and C6 also reduce any noise that may be introduced by spurious from the power supply. Normal values for C5 and C6 would be 0.1 μF or 1 μF.

Resistor R5 is commonly used in some LNA designs to reduce in-band gain and improve stability.

Bias Networks

One of the major advantages of the enhancement mode technology is that it allows the designer to be able to DC ground the source leads and then merely apply a positive voltage on the gate to set the desired amount of quiescent drain current I_{DS}. As a result there are no power supply sequencing concerns as there would be with depletion mode FETs.

Whereas a depletion mode PHEMT pulls maximum drain current when V_{GS}=0 V, an enhancement mode PHEMT pulls only a small amount of leakage current when V_{GS}=0 V. Only when V_{GS} is increased above V_{TO}, the device threshold voltage, will drain current start to flow. At a V_{DS} of 3 V and a nominal V_{GS} of 0.58 V, the drain current I_{DS} will be approximately 20 mA. The data sheet suggests a minimum and maximum V_{GS} over which the desired amount of drain current will be achieved. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals.

Passive Biasing

The LNA shown in Figure 1 uses passive biasing. A voltage divider consisting of R1 and R2 provides the voltage necessary at the gate of the device. The voltage for the divider is derived from the drain voltage. This provides a form of voltage feedback (through the use of R3) to help keep drain current constant. Besides providing the proper gate voltage, R1 and R2 should also be selected to limit the gate current drawn by the VMMK-1218. Under normal class A conditions, the gate current is only a few microamperes. As the device is being driven close to 1 dB gain compression point and beyond, the gate will begin to conduct. The maximum safe gate current is a function of device gate width. A rule of thumb would be to limit the gate current to less than 4 mA for 1000-micron gate width. For the 400-micron gate width VMMK-1218 the maximum safe gate current would then be 1.6 mA.

Resistor R3 is calculated based on the desired V_{DS}, I_{DS} and available power supply voltage.

$$R3 = \frac{V_{DD} - V_{DS}}{I_{DS} + I_{BB}} \qquad (1)$$

V_{DD} is the power supply voltage

V_{DS} is the device drain-to-source voltage

I_{DS} is the desired drain current

I_{BB} is the current flowing through the R1/R2 resistor voltage divider network.

If resistor R5 is used then the voltage drop across R5 must be taken into account when calculating R3.

The value of resistors R1 and R2 are calculated with the following formulas.

$$R1 = \frac{V_{GS}}{I_{BB}} \qquad (2)$$

$$R3 = \frac{(V_{DS} - V_{GS}) \cdot R1}{V_{GS}} \qquad (3)$$

As an example, the following conditions are used.

V_{DD}=5 V

V_{DS}=3 V

I_{DS}=20 mA

V_{GS}=0.58 V

We will pick the current I_{BB} through the voltage divider to be 400 μA. When the VMMK-1218 is driven into compression, the gate will start to forward conduct causing the device to want to sink current from the voltage source. If we want to limit the current drawn from the power supply then we must limit the current (I_{BB}) through R2 to be 400 μA.

Using equations (1), (2), and (3) the resistors are calculated as follows

R1=1450 Ω

R2=6050 Ω

R3=98 Ω

Using the ADS Root Model for the VMMK-1218, the bias circuit was analyzed with respect to its ability to limit gate current under RF drive compression. A graph of gate current vs RF drive level shown in Figure 2 shows an interesting property. As the RF drive level is increased up to about +5 dBm, resistor R2 is limiting the gate current to something less than 20 μA. As the power is increased to +10 dBm, the gate to source junction is starting to conduct even harder because the RF drive level is beginning to self bias the gate to source junction increasing the gate current to upwards of 300 μA which is still quite a bit less than the maximum suggested gate current of 1.6 mA.

Active Bias

Active biasing provides a means of keeping the quiescent bias point constant over temperature and constant over lot to lot variations in device DC performance. The advantage of the active biasing of an enhancement mode PHEMT versus a depletion mode PHEMT is that a negative power source is not required. The techniques of active biasing an enhancement mode device are very similar to those used to bias a bipolar junction transistor.

An active bias scheme is shown in Figure 3. A general purpose dual PNP transistor is used in the regulator. Q2b is wired solely as a diode to offset the V_{BE} changes in Q2a over temperature. R2 and R3 provide a constant voltage source at the base of Q2a. The constant voltage at the base of Q2a is raised by 0.7 V at the emitter. The difference between the constant emitter voltage and the regulated V_{DD} supply is present across resistor R4. Constant voltage across R4 provides a constant current supply for the drain current. Resistors R2 and R3 are used to set the desired V_{DS} which is the same as the emitter voltage on Q2a unless an additional resistor R5 is used in the circuit. The combined series value of R2 and R3 also sets the amount of extra current consumed by the bias network.

The equations that describe the circuit's operation are as follows.

$$V_E = V_{DS} + (I_{DS} \cdot R5) \quad (1)$$

$$R4 = \frac{(V_{DD} - V_E)}{I_{DS}} \quad (2)$$

$$V_E = \frac{R2}{R2 + R3} \cdot V_{DD} \quad (3)$$

$$V_{DD} - V_{BE} = I_{BB} (R2 + R3) \quad (4)$$

Rearranging equations (3) and (4) provides the following formula

$$R2 = \frac{V_E \cdot (V_{DD} - V_{BE})}{V_{DD} \cdot I_{BB}} \quad (5)$$

and rearranging equation (4) provides the follow formula

$$R3 = \left(\frac{V_{DD} - V_{BE}}{I_{BB}} \right) - R2 \quad (6)$$

As an example, the following conditions are used.

V_{DD}=5 V

V_{DS}=3 V

I_{DS}=20 mA

V_{BE}=0.7 V

R5 = 0 Ω

The current I_{BB} through the voltage divide is chosen to be 5% of the desired drain current, therefore I_{BB} = 1 mA. Equation (1) calculates the increased voltage required if resistor R5 is used. If R5 is zero then $V_E = V_{DS}$. Equation (2) calculates the value of resistor R4 which is used to set the desired drain current I_{DS}. Equations (3) and (4) describe the voltage divider that produces the voltage required to force the desired drain voltage V_{DS}. The dual PNP transistor provides both regulation and temperature compensation. Equations (3) and (4) are solved simultaneously to determine the value of resistors R1 and R2 shown in equations (5) and (6).

Solving the equations produces the following resistor values.

R2 = 6450 Ω

R3 = 4300 Ω

R4 = 100 Ω

Resistor R1 is chosen to be 10 kΩ to help keep some current flowing through Q2a to help maintain regulation. Resistor R7 is chosen to be 10 kΩ to limit the gate current when the device is subjected to high RF drive levels. C7 provides a low frequency bypass to keep noise from Q2 effecting the operation of Q1. C7 is typically 0.1 μF. Resistor R4 is also dual purpose in that it also provides the low frequency resistive termination for the VMMK-1218.

Printed Circuit Board Material and Thickness

Choosing the proper printed circuit board thickness is as important as the circuit design itself. Besides providing the mechanical rigidity, good thermal properties and low loss, the printed circuit board thickness directly relates to and is an important parameter in determining amplifier stability.

Most amplifier designs use microstrip for matching and bias decoupling. The microstrip achieves its characteristics by working in conjunction with a grounplane that is some small distance below the microstrip etch. The field that is set up with the groundplane helps to establish the micrsotrip's characteristic impedance. Its characteristic impedance and electrical length provide the basis for impedance matching. This same groundplane should be continuous from the amplifier input port or connector to its output port or connector.

The FET must also use this same groundplane as its reference. Since the FET is generally mounted on the top side of the printed circuit board, then any electrical length between the device source lead or leads and the groundplane can have an effect on the device performance. Most FETs like the Avago ATF-36077 and the ATF-5XXX family, have two source leads that must be grounded properly for best operation. In the case of the VMMK-1218, there is only one source terminal which is actually a small slab of copper on the bottom of the device. The gate and drain are connected to the appropriate input and output matching networks. Generally, the source pad is connected to the bottom groundplane through a series of plated through holes. Given the physical size of the VMMK-1218, only two plated through holes of 0.010 inch in diameter are used. The thickness of the printed circuit board represents a fixed amount of inductance that is in series with the source lead of the FET. However small the thickness of the printed circuit board may seem, its effect on amplifier performance and most importantly stability is significant.

In ADS, the effect of the printed circuit board can be simulated by modeling the thickness of the PCB as two vias of 0.010 inch in diameter and their length being equal to the printed circuit board thickness. A simple S-parameter analysis is performed on the VMMK-1218 with 2 plated through holes in series with the source. The VMMK-1218 is biased at a V_{DS} of 3 V with I_{DS} of 20 mA. Figure 4 shows the 50 Ω gain for varying printed circuit board thicknesses. At a 0.005 inch thickness, the gain is at its maximum at low frequencies. As the printed circuit thickness is increased to 0.030 inch, the low frequency gain decreases. Although not specifically shown in Figure 4, the gain at frequencies above 18 GHz will increase with increasing source inductance. In short, adding source inductance makes the FET degenerative at low frequencies and regenerative at higher frequencies. Although this "control" on FET gain may seem attractive for adjusting FET gain, it does have other important side effects. The most important of which is stability. It is customary to calculate the Rollett stability factor K or the more recently accepted factor called mu. Having K or mu greater than or equal to 1 over all frequencies indicates unconditional stability. Both K and mu are calculated in ADS over a broad range from 100 MHz to 18 GHz. The results of which are shown in Figure 5 for various printed circuit board thicknesses. Keep in mind that a discrete FET can not be expected to be unconditionally stable without proper circuit design. Generally resistive loading and some amount of shunt or series feedback can make a FET amplifier stable. In fact some amount of source inductance can be beneficial to a well designed FET circuit up to a point. The point of "too much" is fairly easy to determine by careful analysis of Figure 5. As the printed circuit board thickness is increased beyond about 0.020 inch, both K and mu start to dip below 1 at 18 GHz and higher. Thicker printed circuit board thicknesses may very well be possible. However, only with careful circuit analysis will actual performance be predictable. Lossy elements such as lossy printed circuit board material and resistive elements in shunt or series can often be used to enhance stability even further with thicker printed circuit boards.

Based on this analysis the maximum suggested printed circuit board thickness for the VMMK-1218 is 0.020 inch with 0.008 or 0.010 inch being the maximum preferred thickness. Thicker printed circuit boards may cause stability issues at 18 GHz and higher. In some cases, a small amount of source inductance in the form of 0.010 inch source leads could be added to 0.010 inch printed circuit board to help with stability. This concept will be covered in future application notes. In all situations, a careful stability analysis should be performed. Any instability regardless of the frequency can render any FET useless even if the intended operation is at 2 GHz and the potential instability is at 18 GHz .

For further Information

The information presented here is an introduction to the use of the VMMK-1218 enhancement mode PHEMT. More detailed application circuit information is available from Avago Technologies. Consult the web page or your local Avago Technologies sales representative.

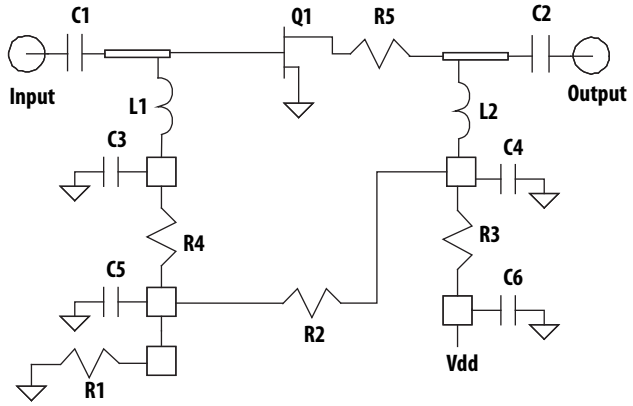

Figure 1. Typical VMMK-1218 LNA using passive biasing.

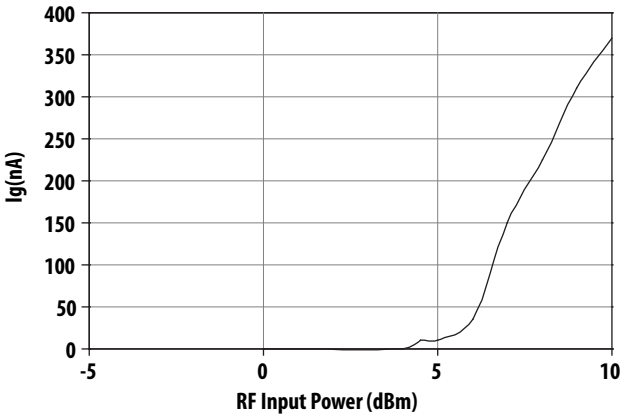

Figure 2. Gate current vs RF drive level for the VMMK-1218

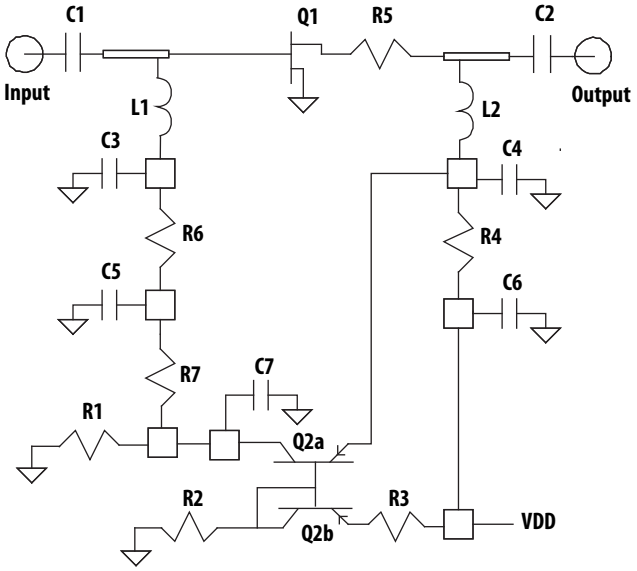

Figure 3. Active biasing the VMMK-1218

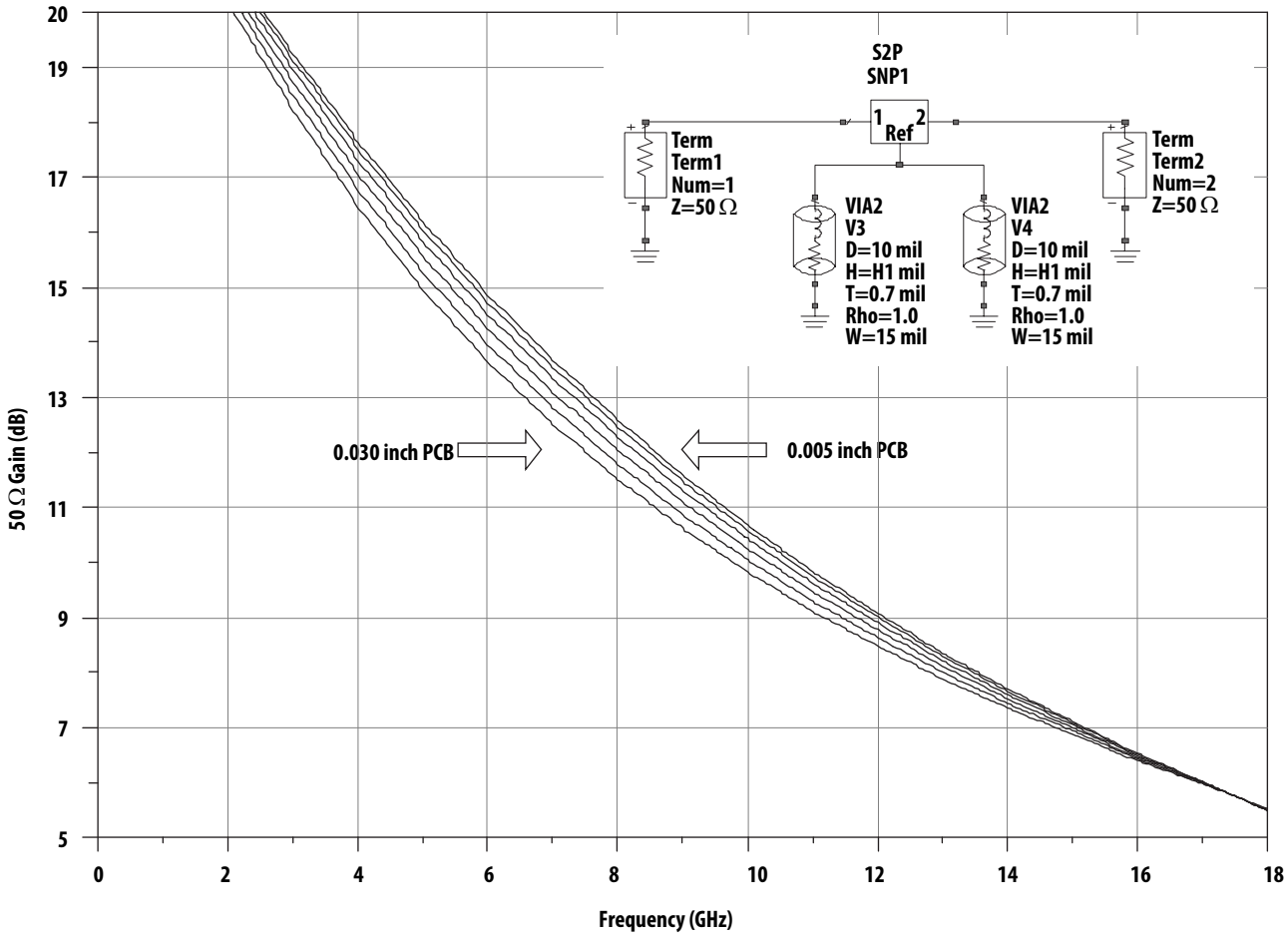

Figure 4. VMMK-1218 50 Ω gain vs frequency for varying printed circuit board thickness

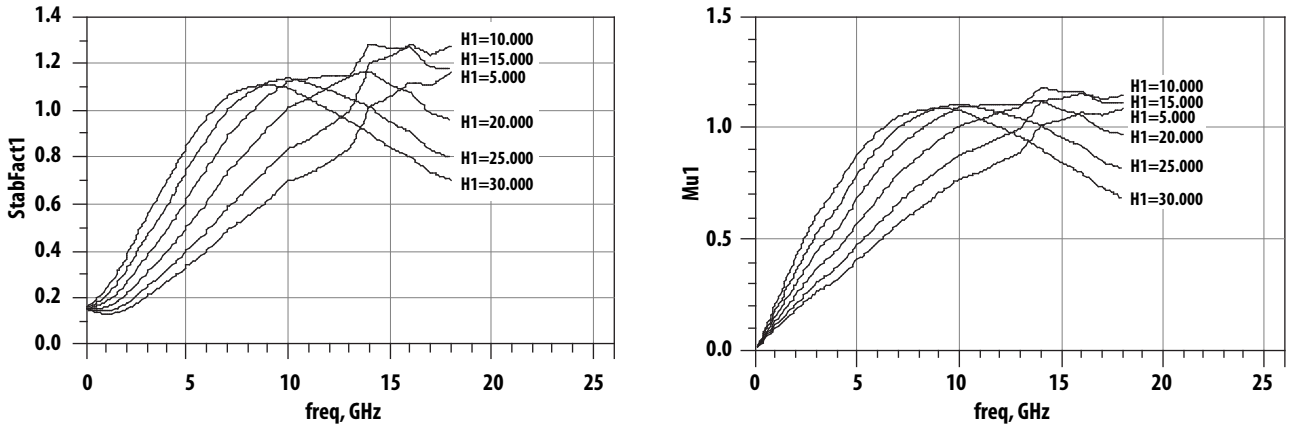

Figure 5. Stability analysis of the VMMK-1218 at Vds =1.5 V and Ids = 20 mA versus printed circuit board thickness on 1000'ths of an inch

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